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CmpE 110 Lab 5: CMOS & TTL Interfacing

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*Abstract*— The goal in this lab is to determine a base resistor and a collector resistor for an npn transistor such that a CMOS inverter can drive a TTL inverter and vice versa within constraints.

# INTRODUCTION

The purpose of this lab is to find a base resistor and a collector resistor for an npn transistor such that a CMOS inverter can drive a TTL inverter and vice versa. This analysis requires an examination of the various constraints both devices operate by, such as output current, input current, and voltages. This experiment also examines whether the transistor is operating in saturation or cut-off region depending on what logical signal the driver is outputting.

# Design methodology

## Parts List

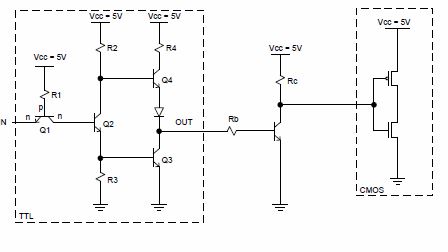
* SN7404 TTL inverter
* CD4069 CMOS inverter
* 2N3904 npn bipolar transistor
* 5 V DC power source
* Tektronix AFG3021B Function Generator
* Tektronix DPO3032 Oscilloscope

## Original and Derived Equations

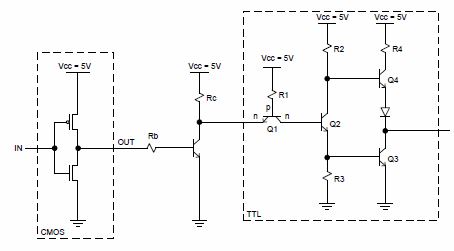
CMOS to TTL Example:

@ Ic = 30 mA (from Chart 1):

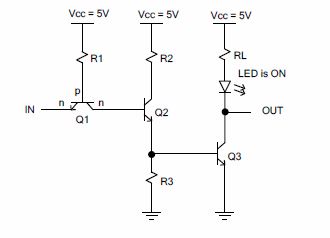
## Schematics



*Schematic 1. TTL inverter driving CMOS inverter through bipolar transistor*



*Schematic 2. CMOS inverter driving TTL inverter through bipolar transistor*



*Schematic 3. Open collector TTL inverter driving an LED*

# Testing Procedures

In performing this experiment, a 5 V square wave is the input signal of a TTL inverter.

1. Tie the output of the driving inverter to the base of the bipolar transistor through a resistor Rb.
2. Tie the collector of the transistor to Vcc through a resistor Rc and the input of inverter being driven.
3. Calculate the values of Rb and Rc such that the electrical characteristics such as VOH, IOH, VOL, IOH, IIH, and IIL are satisfied.
4. Perform step 3 for when the driving inverter is outputting a H signal and then outputting a L signal.
5. Verify the output waveform of the driven inverter with the oscilloscope.
6. Repeat steps 1-5 for a CMOS inverter driving a TTL inverter.

# testing results/calculations

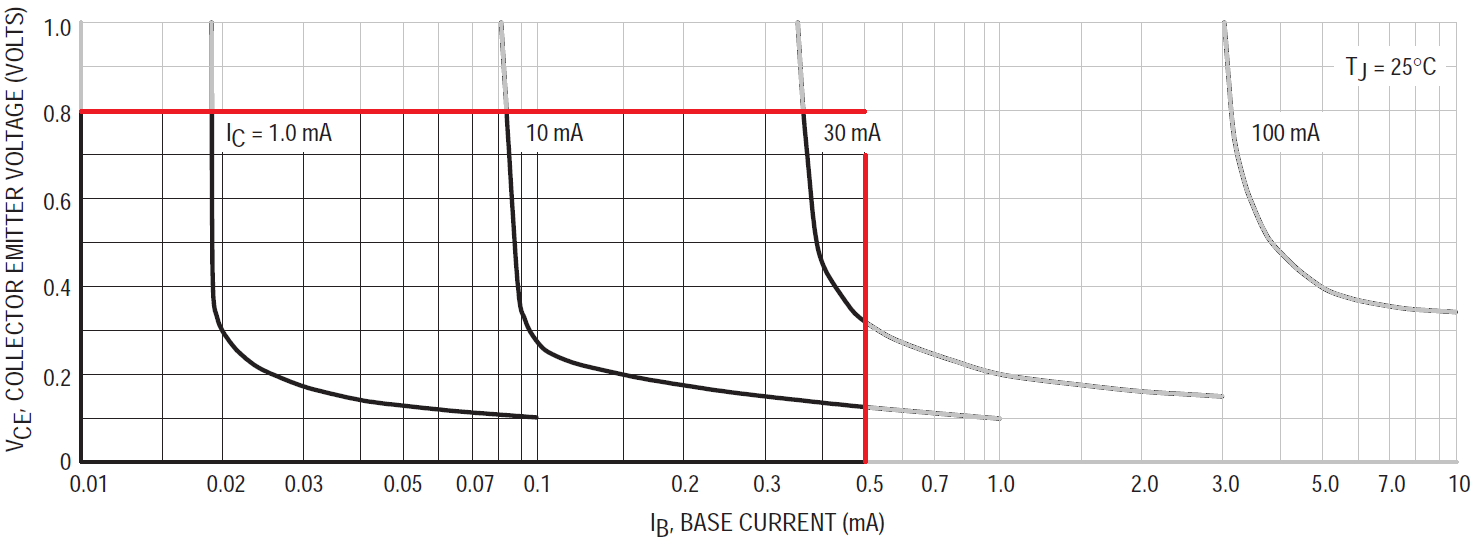
In the case of the TTL inverter driving a CMOS inverter when it's outputting a H signal, the electrical constraints of VOHttl = 2.4 V and IOH = 0.4 mA had to be followed for the base of the transistor. As seen in the example calculation above we found that an Rb of 8.2 K-Ohms and an Rc of 160 Ohms will provide the proper level shifting. As for the LED characteristic resister, we could simply use a 390 Ohm resister to get a decent level of brightness while still limiting the LED’s current to an acceptable level.

# Conclusion

In this lab, we learned about level shifting for various CMOS/TTL configurations. In addition we learned how to deal with CMOS 3.3V and TTL 5V interfacing. Lastly, we learned how to interface logic devices with user interface tools like LEDs. In reality, the datasheets we had available for our devices (linked below) were difficult to read. For instance, in class we learned how to read Ic vs Vce charts with various Ib curves drawn on it. However, the charts in the datasheet were presented as Ib vs Vce charts with Ic curves. To compensate for this we forwent using a load line and instead used bounding boxes as you can see in Chart 1.

# appendices and references

(See next page.)



*Chart 1. Collector Saturation Region of 2N3904*

References:

<http://www.mit.edu/~6.301/2N3904o.pdf>

<http://www.ti.com/lit/ds/symlink/sn7404.pdf>

<http://www.onsemi.com/pub/Collateral/MC14069UB-D.PDF>

1. Farbod Jahan, Anahit Sarao [↑](#footnote-ref-1)